Ser. No. 10/069,200 Amdt. dated August 5, 2005 Reply to Office action of April 18th, 2005

## **Amendments to the Claims**

This listing of claims will replace all prior versions, and listings, of claims in the application:

## **Listing of the Claims**

Claims 1-24 (cancelled)

- 25. (new) A tuner comprising:
  - a first storage means for storing alignment data for said tuner;
  - a first control means including a phase-locked loop coupled to said first storage means for accessing alignment data wherein:
  - said first control means utilizes said alignment data in performing tuner specific algorithms in response to a control signal from a second control means.
- 26. (new) The tuner of claim 25 wherein said first control means is a phase-locked loop integrated circuit.
- 27. (new) The tuner of claim 26 wherein said first storage means is a first non-volatile memory.
- 28. (new) The tuner of claim 27 wherein the first storage means is an EEPROM...
- 29. (new) The tuner of claim 27 wherein said first nonvolatile memory is integrated into said phase-locked loop integrated circuit.
- 30. (new) The tuner of claim 25 wherein the tuner further comprises a D/A converter.
- 31. (new) The tuner of claim 25 wherein the tuner further comprises an address decoder.
- 32. (new) The tuner of claim 31 wherein the address decoder includes a 1 to 1 actual channel to alignment addressing scheme.
- 33. (new) The tuner of claim 31 wherein the address decoder includes a plurality to 1 actual channel to alignment channel addressing scheme.
- 34. (new) The tuner of claim 31 wherein the address decoder is implemented using software.
- 35. (new) The tuner of claim 31 wherein the address decoder is implemented using hardware.
- 36. (new) The tuner of claim 25 wherein said first control means is coupled to said second control means via an inter-integrated circuit bus.